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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,610	04/14/2005	Laurent Regnier	S1022.81223US00	8399

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EXAMINER	
FONG, VINCENT	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,610	REGNIER, LAURENT	
	Examiner	Art Unit	
	Vincent Fong	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4-14-2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4-14-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 04-14-2005.

Claims 1-8 are pending and have been examined.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. Cite number 15-17 in the information disclosure statement filed 4-14-05 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

3. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code (page 2 line 14). Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Claim Objections

4. Claims 1, 4-5 and 8 are objected to because of the following informalities:

As per claim 1, "0A" (line 1) should be changed to "A". In addition limitation "the chip" lack antecedent basis and it should be changed to "a chip".

As per claim 4, the meaning of the term "a predetermined number of output terminals" is unclear, it should be changed to "a predetermined number of coding output terminals".

As per claim 5, the meaning of the term "certain types of instruction only are" is unclear, it should be changed to "only certain types of instruction are".

As per claim 8, the limitation "the state" lack antecedent basis and it should be changed to "state".

Appropriate correction is required.

5. Claim 7 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The parent claim (claim 1) of claim 7 includes the limitation of "monitoring device integrate on a chip of a microprocessor" which cover the limitation of claim 7 "integrated circuit comprising a microprocessor and the monitoring device" since a chip is an integrated circuit.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-3 and 6-8 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/535064 in view of Trauben (USPN 5594864).

As per claim 1, 064' claim 1 discloses:

A monitoring device integrated on a chip of a microprocessor executing a sequence of instructions (line 1-3), comprising: a message calculation means for, on each execution of an instruction from among a plurality of instructions of predetermined types, generating a digital message corresponding to the executed instruction (line 5-10); a buffer memory for storing each generated message (line 12-16).

064' does not discloses a plurality of output terminals each output terminal being associated with one of the instruction types and the message calculation means

modifying the state of the output terminal associated with an instruction type at the time when a message corresponding to said instruction type is stored in the buffer memory. However, Trauben discloses a monitor (element 50 figure 5) collect processor information (column 8 line 17-20) and a plurality of output terminals (element 51 figure 5), in which each output terminal being associated with one of the instruction types [8 types of instruction (column 9 line 50 – column 10 line 7) and the message calculation means (element 50 figure 5) modifying the state of the output terminal associated with an instruction type at the time when an instruction corresponding to said instruction type is executed [generate the signal on corresponding output port according to the upon the information of execution in the processor (Trauben column 8 line 26-30) is collected, which is also the same time in 064' system generate and store message].
It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include pluarity of output terminal associated to a instruction type and modify the state of output when the corresponding instruction type was executed in the processor in the system of 064' because Trauben teach that the inclusion would enable the observation of important processor internal state in a cycle by cycle basis (Trauben column 8 line 26-30).

As per claim 2, the rejection of claim 1 is incorporated and 064' claim 1 further discloses:

the buffer memory is divided into several areas each of which is associated with a different instruction type and is intended to only store messages associated with said instruction type (line 12-16).

As per claim 3, the rejection of claim 1 is incorporated and Trauben further discloses: each output terminal (element 51 figure 5) is connected to a test terminal (element 55 figure 5) (column 8 line 23-26).

As per claim 6, the rejection of claim 1 is incorporated and Trauben further discloses: each of the possible instruction types is associated with an output terminal of the message calculation means (each type of instruction that is monitored will be represent by a PIPE signal (column 8 line 30 – column 9 line 7)].

As per claim 7, the rejection of claim 1 is incorporated and 064' claim 1 further discloses:
An integrated circuit (the chip) comprising a microprocessor and the monitoring device (line 1-3).

As per claim 8, see similar rejection of claim 1.

8. Claim 4 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over 064' claim 1 in view of Trauben as applied

to claim 1 above, and further in view of Mihalik et al. (USPN 4574354, hereinafter Mihalik).

As per claim 4, the rejection of claim 1 is incorporated and the combination of 064' claim 1 and Trauben discloses the limitations of claim 1.

Neither 064' claim 1 nor Trauben discloses a coding block.

However Mihalik discloses each output terminal (TTA, element 12C figure 1) is connected to an input terminal of a coding block (element 16) comprising a predetermined number of coding output terminals each of which is connected to a test terminal (element 14) [each bit of the output of a grey code counter is a output terminal of the coding block (column 7 line 53-57)] each coding block being provided to have each of its n output terminals switch once every n state switchings of its input terminal (pulse emitted by TTA) and so that a single one of its n output terminals switches state at once [the use Grey code (column 7 line 53-57)].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include encode state change in the output terminal by Gray code to be a encoded number in the system of 064' and Trauben because it is encoded the number of the time the state of input terminal change into a count (Mihalik column 7 line 53-57).

9. Claim 5 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over 064' claim 1 in view of Trauben as applied

to claim 1 above, and further in view of Yamashita et al. (USPN 6467083, hereinafter Yamashita).

As per claim 5, the rejection of claim 1 is incorporated and the combination of 064' claim 1 and Trauben discloses the limiations of claim 1.

Neither 064' claim 1 and Trauben discloses only certain types of instruction are associated to an output terminal.

However, Yamashita discloses Only certain types of instructions are associated with an output terminal of the message calculation means [tracing condition can be specified, not all type of instruction will generate a tracing packet and further be associated to an output terminal to be sent out (column 8 line 48-50)].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to make only certain type of instruction are associated with an output terminal in the system of 064' and Trauben because only instruction of interest is monitored (Yamashita column 7 line 66 – column 8 line 3).

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claim 1,3 and 5-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (USPN 6467083) in view of Trauben (USPN 5594864).

As per claim 1, Yamashita discloses:

A monitoring device (element 16 figure 3) integrated on a chip of a microprocessor (element 12 figure 3) executing a sequence of instructions, comprising: a message calculation means (element 22 figure 3) for, on each execution of an instruction from among a plurality of instructions of predetermined types [information of the execution is provided by the data selector (column 8 line 8-19)], generating a digital message (trace packer) corresponding to the executed instruction [packet generator generate trace packet according to the information provided by the data selector, different type of packet is generated depending on the type of instructions (column 8 line 20-25)]; a buffer memory (element 17 figure 3) for storing each generated message (column 7 line 43-46); and a output terminal (element 24 figure 3) connected to an external analysis tool (element 13 figure 3).

Yamashita does not discloses a plurality of output terminals each output terminal being associated with one of the instruction types and the message calculation means

modifying the state of the output terminal associated with an instruction type at the time when a message corresponding to said instruction type is stored in the buffer memory. However, Trauben discloses a monitor (element 50 figure 5) collect processor information (column 8 line 17-20) and a plurality of output terminals (element 51 figure 5), in which each output terminal being associated with one of the instruction types [8 types of instruction (column 9 line 50 – column 10 line 7) and the message calculation means (element 50 figure 5) modifying the state of the output terminal associated with an instruction type at the time when an instruction corresponding to said instruction type is executed [generate the signal on corresponding output port according to the upon the information of execution in the processor (Trauben column 8 line 26-30) is collected, which is also the same time in Yamashita's system generate and store trace packer]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include pluarity of output terminal associated to a instruction type and modify the state of output when the corresponding instruction type was executed in the processor in the system of Yamashita because Trauben teach that the inclusion would enable the observation of important processor internal state in a cycle by cycle basis (Trauben column 8 line 26-30). It enhances the ability of Yamashita's system to collect important trace information in real time (Yamashita column 5 line 21-24).

As per claim 3, the rejection of claim 1 is incorporated and Trauben further discloses: each output terminal (element 51 figure 5) is connected to a test terminal (element 55 figure 5) (column 8 line 23-26).

As per claim 5, the rejection of claim 1 is incorporated and Yamashita further discloses: only certain types of instructions only are associated with an output terminal of the message calculation means [tracing condition can be specified, not all type of instruction will generate a tracing packet and further be associated to an output terminal to be sent out (column 8 line 48-50)]

As per claim 6, the rejection of claim 1 is incorporated and Trauben further discloses: each of the possible instruction types is associated with an output terminal of the message calculation means (each type of instruction that is monitored will be represent by a PIPE signal (column 8 line 30 – column 9 line 7)].

As per claim 7, the rejection of claim 1 is incorporated and Yamashita further discloses: An integrated circuit (element 12 figure 3) comprising a microprocessor (element 15 figure 3) and the monitoring device (element 16 figure 16).

As per claim 8, see similar rejection of claim 1.

13. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Trauben as applied to claim 1 above, and further in view of Chen et al. (USPN 5642478, hereinafter Chen).

As per claim 2, the rejection of claim 1 is incorporated and Yamashita discloses:

The buffer memory (element 17 figure 3).

Neither Yamashita nor Trauben discloses the division on buffer memory and association of memory part with certain instruction type.

However Chen discloses the buffer memory (element 32 figure 1) is divided into several areas (element 56 figure 1) each of which is associated with a different instruction type and is intended to only store messages associated with said instruction type (column 9 line 23-26).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include different areas in the buffer memory and each associated to each instruction type in the system of Yamashita and Trauben because Chen teach that the inclusion would enable the correlation of trace data from different source(Chen Column 9 line 1-2). It enhances the capability of the accumulation of trace data information by organization of the information in the storage (Yamashita column 5 line 21-24).

14. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Trauben as applied to claim 1 above, and further in view of Mihalik et al. (USPN 4574354, hereinafter Mihalik).

As per claim 4, the rejection of claim 1 is incorporated and the combination of Yamashita and Trauben discloses the limitations of claim 1.

Neither Yamashita nor Trauben discloses a coding block.

However Mihalik discloses each output terminal (TTA, element 12C figure 1) is connected to an input terminal of a coding block (element 16) comprising a

predetermined number of coding output terminals each of which is connected to a test terminal (element 14) [each bit of the output of a grey code counter is a output terminal of the coding block (column 7 line 53-57)] each coding block being provided to have each of its n output terminals switch once every n state switchings of its input terminal (pulse emitted by TTA) and so that a single one of its n output terminals switches state at once [the use Grey code (column 7 line 53-57)].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include encode state change in the output terminal by Gray code to be a encoded number in the system of Yamashita and Trauben because it is encoded the number of the time the state of input terminal change into a count (Mihalik column 7 line 53-57). It enhances the capability of the accumulation of trace data information by collecting more information (the count of certain type of instruction executed in the processor) (Yamashita column 5 line 21-24).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Swaine et al. (UPSN 7080289) discloses an on chip trace circuit and a buffer to store trace data and Site et al. (USPN 5764885) discloses on chip trace circuit, a buffer to store trace data and output terminal that line with an external analyzer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on 7:00-3:30 Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Fong VF
March 15 2007

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